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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/678,751 | 10/03/2000 | John B. Halbert | 5038-63 | 5518 |

20575 7590 08/05/2003

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/678,751 | HALBERT ET AL. | |
| | Examiner | Art Unit | |
| | Pierre M. Vital | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,10-12,14 and 17-25* is/are rejected.

7)☒ Claim(s) *3,6-9,13,15,16,* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed July 2, 2003 in response to PTO Office Action mailed April 25, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-25 have been presented for examination in this application. In response to the last Office Action, claims 10, 11 and 20 have been amended. No claims have been canceled or added. As a result, claims 1-25 are now pending in this application.

3. The objection to the specification has been withdrawn due to the amendment filed July 2, 2003.

4. The rejection of claim 20 under 35 USC 112, second paragraph has been withdrawn due to the amendment filed July 2, 2003.

5. The rejection of claim 3 under 35 USC 103(a) has been withdrawn due to the amendment filed July 2, 2003.

6. The rejection of claims 1-4, 10-12, 14, 17-19 and 21-25 as in the Office Action mailed April 25, 2003 (paper No. 5) is respectfully maintained and reiterated below for applicant's convenience.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 4-5, 14 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham et al. (US6,530,033) and Canfield et al (US5,825,424).

As per claims 1, Raynham discloses a memory system comprising a primary memory controller [Fig. 4A, *memory controller 421*]; a memory data bus, having an effective bit-width *m*, coupled to the primary memory controller [Fig. 4A, *memory data bus 427*]; and at least one memory module coupled to the memory data bus [*memory modules 424;* Fig. 4A, col. 7, lines 44-48].

However, Raynham does not specifically teach a memory module having a module data bus with an effective bit-width $N = R \times m$, where $R$ is an integer value greater than one, the memory module comprising an interface circuit coupled between the memory data bus and the module data bus, the interface circuit capable of performing *m*-bit-wide data transfers on the memory data bus, the interface circuit capable of performing *N*-bit-wide data transfers on the module data bus as recited in the claim.

Canfield discloses a memory module having a module data bus with an effective bit-width $N = R \times m$, where $R$ is an integer value greater than one [*internal bus is 192 bits wide which is a multiple of 96, 64, 48;* col. 6, lines 1-10], the memory module comprising an

interface circuit coupled between the memory data bus and the module data bus [*memory interface 31;* Fig. 12, col. 6, lines 1-2], the interface circuit capable of performing *m*-bit-wide data transfers on the memory data bus [*external bus has bit width of 96, 64 or 48;* col. 6, lines 7-10], the interface circuit capable of performing *N*-bit-wide data transfers on the module data bus [*internal bus is 192 bits wide which is N times external bus width;* col. 6, lines 15-16].

As per claims 5 and 20, Raynham discloses a memory module comprising R ranks of memory devices, where R is at least two [*memory devices 422;* Fig. 4A, col. 8, lines 41-47], each rank having an m-bit wide data port [*memory module bus 460a-460d;* Fig. 4A]; a module data port capable of exchanging data signaling over a memory data bus having an effective bit width m [col. 7, lines 49-50; col. 9, lines 1-5].

However, Raynham does not specifically teach an interface circuit coupled between the module data port and the *R* memory device rank data ports, the interface circuit capable of performing *m*-bit wide data transfers at the module data port, the interface capable of performing R*xm* bit-wide data transfers with the R ranks of memory devices; and a controller capable of synchronizing the operation of the interface circuit and the memory device ranks such that a data transfer comprising *R* serial data transfers on the memory data bus can be completed internal to the memory module with one *Rxm* bit-wide data transfer with the memory device ranks as recited in the claims.

Canfield discloses an interface circuit coupled between the module data port and the *R* memory device rank data ports [*memory interface 31;* Fig. 12, col. 6, lines 1-2], the interface circuit capable of performing *m*-bit wide data transfers at the module data port,

the interface capable of performing *Rxm* bit-wide data transfers with the *R* banks of memory devices [*internal bus is 192 bits wide which is N times external bus width;* col. 6, lines 15-16]; a controller capable of synchronizing the operation of the interface circuit and the memory device ranks such that a data transfer comprising *R* serial data transfers on the memory data bus can be completed internal to the memory module with one *Rxm* bit-wide data transfer with the memory device ranks [*data is multiplexed or demultiplexed to the internal bus width;* col. 6, lines 7-22].

It would have been obvious to one of ordinary skill in the art, having the teachings of Raynham and Canfield before him at the time the invention was made, to modify the system of Raynham to include a memory module having a module data bus with an effective bit-width $N = R \times m$, where *R* is an integer value greater than one, the memory module comprising an interface circuit coupled between the memory data bus and the module data bus, the interface circuit capable of performing *m*-bit-wide data transfers on the memory data bus, the interface circuit capable of performing *N*-bit-wide data transfers on the module data bus and an interface circuit coupled between the module data port and the *R* memory device rank data ports, the interface circuit capable of performing *m*-bit wide data transfers at the module data port, the interface capable of performing R*xm* bit-wide data transfers with the R ranks of memory devices; and a controller capable of synchronizing the operation of the interface circuit and the memory device ranks such that a data transfer comprising *R* serial data transfers on the memory data bus can be completed internal to the memory module with one *Rxm* bit-wide data

transfer with the memory device ranks because it would have provided better memory management and data reduction by varying the data bit width of the external memory path as a function of the memory size [col. 15, lines 29-32] as taught by Canfield.

As per claim 2, Raynham discloses a memory data bus comprising a point-to-point bus having one data bus segment connecting the primary memory controller and the first of the at least one memory modules, and one additional segment for each additional memory module, the additional segment connecting the additional memory module to the module immediately preceding it [col. 5, lines 55-64].

As per claims 4 and 22, Canfield discloses a memory data bus and a module data bus each having a clock rate, the memory data bus clocking at a rate R times the clock rate of the module bus [*internal bus clock rate is less than external bus clock rate;* col. 6, lines 29-33].

As per claim 14, Raynham discloses a module data port comprising a dual-port buffer, each port of the dual-port buffer capable of connection to another memory module in a point-to-point configuration of memory data bus segment [col. 9, lines 19-59].

As per claim 21, Canfield discloses $N = Rxm$ , such that for $R$ data segments transferred between the memory controller and the memory module, one transfer occurs between the interface circuit and the memory devices [col. 6, lines 11-20].

9. Claims 10-12, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham et al. (US6,530,033) and Canfield et al (US5,825,424) and further in view of Osaka et al. (US6,034,878).

As per claim 10, the combination of Raynham and Canfield discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Raynham and Canfield does not specifically teach data transfers between one of the data registers and the corresponding rank of memory devices occurs at a clock rate related to the clock rate of the memory data bus by a factor *1/R* as recited in the claim.

Osaka discloses data transfers between one of the data registers and the corresponding rank of memory devices occurs at a clock rate related to the clock rate of the memory data bus by a factor *1/R* [*equal propagation time, same timing;* col. 2, lines 9-18].

As per claim 11, the combination of Raynham and Canfield discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Raynham and Canfield does not specifically teach a dual-in-line memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus as recited in the claim.

Osaka discloses a dual-in-line memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus [*memory modules 10-0...10-15 using linking connector C3;* Fig. 2; col. 9, lines 50-56].

It would have been obvious to one of ordinary skill in the art, having the teachings of Raynham and Canfield and Osaka before him at the time the invention was made, to modify the system of Raynham and Canfield to include a dual-in-line memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus because it would have provided an improved memory controller by allowing signals propagated from the memory controller to any of the memory modules to have the same waveform and equal propagation time [col. 2, lines 11-13] as taught by Osaka.

As per claim 12, Osaka discloses one of the two ranks of memory devices arranged on each side of the circuit board and connected to the corresponding data register via a set of module data signaling lines routed on the circuit board [*signal lines from the second connector C2-1 of the first memory-module assembly unit U1 to the first connector C1-2 of the second memory-module assembly unit U2 are provided;* Fig. 9, col. 17, lines 35-46].

As per claim 17, Osaka discloses data exchanges over the memory data bus comprise a data strobe signal, the module further comprising a data strobe circuit to generate data strobe signaling when transmitting data over the memory data bus [col. 10, lines 39-43].

As per claim 18, Osaka discloses the controller begins an internal sequence of interface circuit write operation in response to an externally supplied data strobe signal [col. 1, lines 46-52; col. 13, lines 39-42].

As per claim 19 Osaka discloses data exchanges between the interface circuit and the ranks of memory devices comprise a data strobe signal, the module further comprising a data strobe circuit to generate data strobe signaling when transmitting data from the interface circuit to the ranks of memory devices [col. 1, lines 46-52], the interface circuit comprising a register circuit to latch data from the ranks of memory devices based on data strobe signaling received from those devices [col. 13, lines 39-42].

***Allowable Subject Matter***

10. Claims 3, 6-9, 13, 15-16 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or suggest an interface circuit comprising R m-bit wide data registers, each register capable of exchanging point-to-point data signaling with a corresponding rank of memory devices through the data port of that rank; and a multiplexer having a multiplexing ration R, coupled between the R data registers and the external port;

An interface circuit comprising two interface circuits each serving half of the module data port and half of each rank of memory devices in combination with the other elements set forth in the claimed invention.

***Response to Arguments***

12. Applicant's arguments filed July 2, 2003 have been fully considered but they are not persuasive. As to the remarks, applicant asserted that:

(a) Canfield's "internal memory bus" cannot be "coupled to the primary controller".

Examiner respectfully traverses applicant's arguments for the following reasons. Applicant's arguments that Canfield's "internal memory bus" cannot be "coupled to the primary controller" are clearly erroneous.

It should be borne in mind that, in discussions of electrical components, the terms "connected", "operatively connected", "electrically connected", and like terms denote an electrical path between two components. It is understood, however, that such terms do not preclude the existence of additional components interposed between the two original components, even if an additional such component has the capability of interrupting or affecting signal or data transmission between the two original components. Only through the use of the term "directly connected", or like terms, is it intended to denote an electrical connection between two components that precludes any additional components, other than an electrical conductor, interposed between the two original components.

Thus, it can be clearly seen that Canfield's "internal memory bus" can be "coupled to the primary controller" as detailed supra.

(b) Applicant claims an effectively wider bus at the memory while Canfield teaches a narrower bus at the memory.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to emphasize that the memory bus disclosed by Applicant is the same as the (external) memory bus disclosed by Canfield. The claims disclose a memory bus capable of performing m-bit-wide data transfers and a module bus capable of performing N-bit-wide data transfers, where N = Rxm. Canfield discloses an internal (module) bus path being an integer multiple of the (external) memory bus path. It can be clearly seen that the invention as claimed by Applicant and the invention of Canfield both provide a module bus as a multiple of the memory bus. Let's assume that R=2 and m=48 bits, then the module bus bit-width will be N = Rxm = 2 x 48 = 96 bits. The module bus will always be a multiple of the memory bus. Thus, the claimed invention provides for a narrower bus at the memory as detailed by Canfield.

(c) Raynham's system has no "data bus segment connecting the primary memory controller and the first of the at least one memory modules".

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that even though Raynham connects the primary

controller to a central switch, the switch does not preclude the controller from being connected to the memory modules.

It should be borne in mind that, in discussions of electrical components, the terms "connected", "operatively connected", "electrically connected", and like terms denote an electrical path between two components. It is understood, however, that such terms do not preclude the existence of additional components interposed between the two original components, even if an additional such component has the capability of interrupting or affecting signal or data transmission between the two original components. Only through the use of the term "directly connected", or like terms, is it intended to denote an electrical connection between two components that precludes any additional components, other than an electrical conductor, interposed between the two original components.

In view of the above discussion and looking at Fig. 4A, it can be seen that each memory module 424 is connected to the memory module preceding it by the data bus 427. Thus, it can be clearly seen that Raynham provides a "data bus segment connecting the primary memory controller and the first of the at least one memory modules".

(d) Canfield does not teach or suggest "a memory data bus clocking at a rate R times the clock rate of the module data bus".

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that Canfield discloses "the clock rate for the internal

memory (module) path is always less than the external memory path as detailed in column 6, lines 31-33. It can be clearly seen that the clock rate of the internal bus being always less that the clock rate of the (external) memory bus, it can be deduced that the clock rate of the (external) memory bus to be R times the rate of the internal (module) bus.

(e) Canfield's bus to memory is not taught to connect to multiple ranks in parallel.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner would like to point out that Raynham teaches a system where memory modules are connected in parallel as detailed in column 2, lines 14-17. Thus, if the memory modules are connected in parallel, the memory chips affixed to the memory modules, which include the memory banks, and memory ranks must be connected in parallel.

***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
August 1, 2003